The opinion in support of the decision being entered today was not written for publication in a law journal and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DANILO BOJIC

Appeal No. 2005-0834
Application No. 08/897,953

ON BRIEF

Before KIMLIN, OWENS and JEFFREY T. SMITH, Administrative Patent Judges.

KIMLN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 3, 5, 6, 8 and 15-17. Claim 15 is illustrative:

15. A fabrication method of a semiconductor device comprising the steps of:

(a) forming a plurality of projection electrodes on each of a plurality of semiconductor chips;

(b) applying a thermosetting insulating adhesive to areas of mounting parts where the semiconductor chips are to be mounted on a substrate;

(c) heating the thermosetting insulating adhesive on the substrate with a half-thermosetting temperature so as to harden

the thermosetting insulating adhesive to a half-thermosetting state by heating means and, then, aligning the semiconductor chips to the mounting parts of the substrate at a first stage and performing a first fixing of the semiconductor chips with a first pressure by a bonding head to which the semiconductor chips are absorbed;

(d) moving the substrate to a second stage, while the semiconductor chips on the mounting parts of the substrate are held at their position by the half-thermosetting state of the thermosetting insulating adhesive; and

(e) thereafter heating, at the second stage, the substrate, on which the semiconductor chips are fixed, with a thermosetting temperature of the thermosetting insulating adhesive, and performing a second fixing of the semiconductor chips with a second pressure, wherein the second pressure for performing the second fixing of the semiconductor chips is greater than the first pressure for performing the first fixing of the semiconductor chips.

The examiner relies upon the following references as evidence of obviousness:

Fujimoto et al. (Fujimoto)	5,115,545	May 26, 1992
DiStefano et al. (DiStefano)	5,548,091	Aug. 20, 1996
Maeda (Japanese Patent Application)	57-63758	Oct. 21, 1983
Sakata (Japanese Patent Abstract)	4,062,946	Feb. 27, 1992
Koga (Japanese Patent Abstract)	4,302,444	Oct. 26, 1992

Appellants' claimed invention is directed to a method of fabricating a semiconductor device using a thermosetting insulating adhesive on mounting parts where semiconductor chips are to be mounted. The method entails heating the adhesive with

a half-thermosetting temperature, aligning the chips to the substrate at a first stage with a first pressure, moving the substrate to a second stage and heating to a thermosetting temperature while fixing the chips with a second pressure. The second pressure is greater than the first pressure.

The appealed claims stand rejected under 35 U.S.C. § 103(a) as follows:

(a) claims 3, 5, 6, 8 and 15 over the admitted prior art, Maeda and Koga;

(b) claims 3, 5, 6, 8 and 15 over the stated combination of references further in combination with Sakata;

(c) claim 16 over the admitted prior art, Maeda, Koga and DiStefano;

(d) claim 16 over the combination of the admitted prior art, Maeda, Koga and Sakata further in combination with DiStefano;

(e) claim 17 over the admitted prior art in combination with Maeda, Koga and Fujimoto; and

(f) claim 17 over the admitted prior art in combination with Maeda, Koga, Sakata and Fujimoto.

Appellants submit at page 5 of the Brief that "claims 3, 5-6, 8 and 15-17 on appeal should stand or fall together."

We have thoroughly reviewed each of appellants' arguments for patentability. However, we are in complete agreement with the examiner that the claimed subject matter would have been obvious to one of ordinary skill in the art within the meaning of § 103 in view of the applied prior art. Accordingly, we will sustain the examiner's rejections for essentially those reasons expressed in the Answer, and we add the following primarily for emphasis.

There is apparently no dispute that the admitted prior art found in appellants' specification is directed to a method of fabricating a semiconductor device by using a thermosetting insulating adhesive to mount a plurality of semiconductor chips on a substrate. The admitted prior art discussed in the specification does not include first heating the adhesive with a half-thermosetting temperature and applying a first pressure, and then, at a second stage, heating with the thermosetting temperature of the adhesive while applying a second pressure. However, we concur with the examiner that Maeda and Sakata evidence the obviousness of utilizing two heating stages for a bonding adhesive in making electrical devices, and Koga and Sakata support the obviousness of employing a second pressure to permanently affix the bonded components. Maeda teaches that the

initial heating increases the viscosity of the adhesive to prevent the components from shifting before application of the final heating temperature. Also, Sakata teaches bringing the adhesive to a semi-hardened state and testing the operation of the device before applying the final hardening temperature. As for the specific temperatures and pressures to be used at the first and second stages, we totally agree with the examiner that it would be a matter of obviousness for one of ordinary skill in the art to resort to routine experimentation to determine the optimum temperatures and pressures. We simply find no merit in appellants' contention that the "claimed relation between the first and second pressure would require undue experimentation to produce" (page 15 of Brief, second paragraph).

As a final point, we note that appellants base no argument upon objective evidence of nonobviousness, such as unexpected results, which would serve to rebut the prima facie case of obviousness established by the examiner for the claimed subject matter.

In conclusion, based on the foregoing and the reasons well-stated by the examiner, the examiner's decision rejecting the appealed claims is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv) (effective Sep. 13, 2004; 69 Fed. Reg. 49960 (Aug. 12, 2004); 1286 Off. Gaz. Pat. Office 21 (Sep. 7, 2004)).

AFFIRMED

EDWARD C. KIMLIN)
Administrative Patent Judge)
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TERRY J. OWENS) BOARD OF PATENT
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